

# Multi-level storage in phase-change memory: from multi-layer to single layer

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## ABSTRACT

In this paper, we report multi-level storage (MLS) in multi-layer (ML) and single-layer (SL) phase-change memories (PCM). For the former ML-PCM device, the active medium with two layers of chalcogenide consists of a top 30-nm TiN/180-nm SbTeN/20-nm TiN/bottom 120-nm SbTeN stacked multi-layer. Three stable and distinct resistance states are demonstrated in both static and dynamic switching characteristics of the multi-layer devices. For the latter SL-PCM device, the active medium with only one layer of chalcogenide consists of a top 50-nm TiN/150-nm SbTeN. We demonstrate that the number of distinguishable resistance levels can readily reach 16 and even higher. These levels in this study result from the initial threshold switching and the subsequent current-controlled crystallization induced by Joule heating. Therefore, the latter memory allows the creation of many distinct levels, thus enabling the low-cost ultra-high-density non-volatile memory.

**Keywords** Multi-layer, Single-layer, Multi-level storage, Phase-change memory

## INTRODUCTION

There is a rapidly increasing demand for ultra-high-density non-volatile memory (NVM) due to today's explosive proliferation of information. This type of memory can stably store information even if no power is supplied. An extremely attractive characteristic of the future's NVM is multi-level storage (MLS), which is data storage on more than two levels per memory cell; it makes possible a dramatic increase in memory capacity, i.e., much more information can be saved without increasing the cell size. This leads to a decrease in the cost per bit.

Although MLS is very promising for post-flash phase-change memory (PCM) because of the huge available resistance change, few reports on it have been found so far due to the difficulty in practically controlling resistance in PCM.<sup>1-4)</sup> In the past few years, researchers have demonstrated three- and four-level storage based on the layer-by-layer crystallization of chalcogenide films in vertical PCM.<sup>1-2)</sup> However, there is a lack of literatures on MLS in lateral PCMs although lateral PCMs were demonstrated to have many advantages. Here, we report MLS in both a multi-layer PCM and a single-layer lateral PCM with a top heater.

## EXPERIMENTAL METHODS

The current-voltage (I-V) characteristics of the device samples were measured by a semiconductor parameter analyzer (4155B, Agilent Technologies, Ltd.). A waveform generator (Model 2571, Tabor Electronics, Ltd.) was used to apply single pulses to the devices to investigate the programming characteristics.

## RESULTS AND DISCUSSIONS

The phase-change layer of SbTeN is adopted in these devices. SbTeN shows a gradual resistivity drop and good phase stability with increasing annealing temperature, a characteristic which makes it suitable for MLS applications.<sup>5)</sup>

We propose MLS based on multiple phase-change (PC) layers of different thicknesses as shown in Fig. 1. For two PC layers, three levels are expected to be obtained due to the two switchings at two threshold voltages. A top 30-nm TiN/180-nm SbTeN /20-nm TiN/bottom 120-nm SbTeN stacked structure is experimentally adopted as the active medium in the multi-layer devices, as shown in Fig. 2. Three stable and distinct device resistance levels are demonstrated in both static and dynamic switching characteristics of the multi-layer devices, as shown in Figs. 3 and 4. Analysis reveals that two separate crystallization processes causing the two resistance drops could sequentially occur at the steps from the bottom thin 120-nm SbTeN layer to the top thick 180-nm STN layer due to the electric field confinement at the steps as shown in Fig. 5. From the principle and analysis of this ML-PCM, the available number of resistance levels is strictly limited to be  $n+1$  by the number of PC layers  $n$ .

To overcome the above limit, we propose SL-PCM to obtain much more resistance levels as shown in Fig. 6. The active layers of a SL-PCM device consist of 150-nm-thick SbTeN layer with an additional top 50-nm-thick TiN layer. Experimental results, as shown in Fig. 7, exhibit a number of levels up to 16 are distinct and stable, which are induced by electric currents. From Fig. 6(a), the resistance level is dependent on the stop current (programming current), and five levels (from “0” to “4”) are created. By reducing the programming current interval to 0.1 mA, up 16 resistance levels can be readily created. In this case, the MLS results mainly from the gradual enlargement of crystalline region between electrodes by Joule heating according to our analysis. These levels also exhibit good thermal stability as shown in Fig. 8.

## CONCULTIONS

A lateral STN-based PCM with a stacked PC multi-layer was proposed for multi-state storage. Both static and dynamic switching of the prototypical device exhibited three stable resistance states (HR, IR and LR). Analysis based on electric field showed that two resistance switchings with increasing applied voltage successively took place at the lower and upper PC layers, respectively. In SL-PCM, we demonstrated ultra-multiple-level storage based on low-power crystallization using a SbTeN single-layer PCM cell structure. The crystallization induced by Joule heating is non-volatile, low-power and current-driven, and allows ultra-multiple-level storage. This phenomenon is expected to be employed in practical applications to dramatically increase the memory capacity without increasing the cell size.

## REFERENCES

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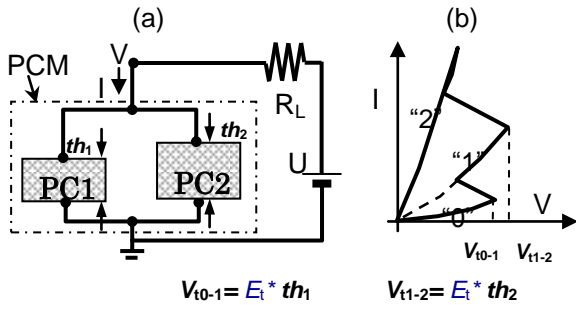


Fig. 1 (a) A proposed multi-level (e.g., three-state) PCM device with two PC layers (PC1 and PC2) of different thicknesses ( $th_1$  and  $th_2$ ). (b) Schematic diagram of I-V curves of the proposed device with three stable levels. Two threshold voltages  $V_{t0-1}$  and  $V_{t1-2}$  are proportional to two thicknesses of  $th_1$  and  $th_2$ , respectively.

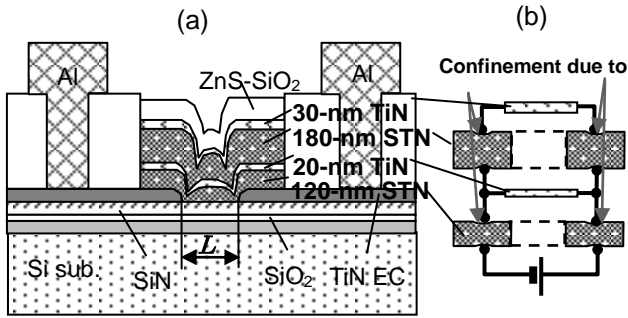


Fig. 2 (a) Schematic diagram of the fabricated phase-change memory device with a stacked multi-layer of top 30-nm TiN/180-nm STN/20-nm TiN/120-nm STN. Gap length and width are  $L$  and  $W$ . (b) Equivalent structure of the fabricated device.

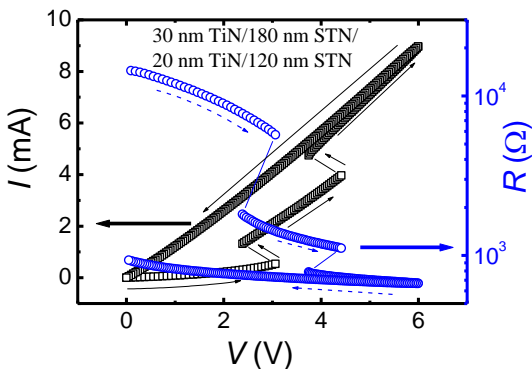


Fig. 3 Current sweeping and R-V characteristics in the multi-layer device. 3 distinct resistance levels were created for 2-layer device.

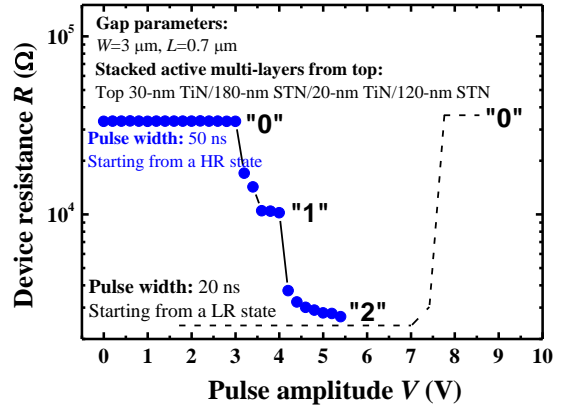


Fig. 4 Pulse-mode dynamic switching characteristics. The HR ("0"), IR ("1") and LR ("2") levels are distinct and stable in a large pulse amplitude window.

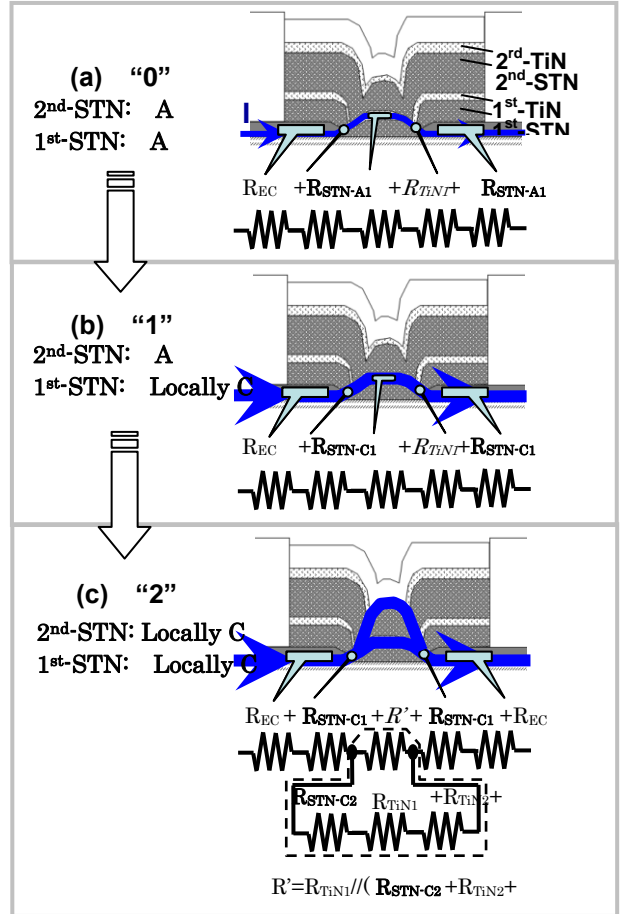
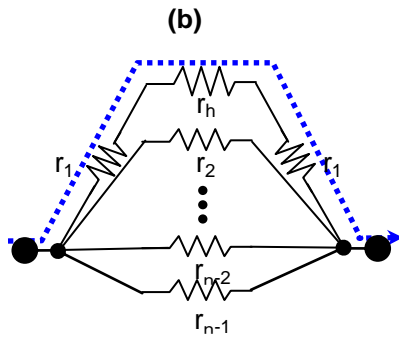
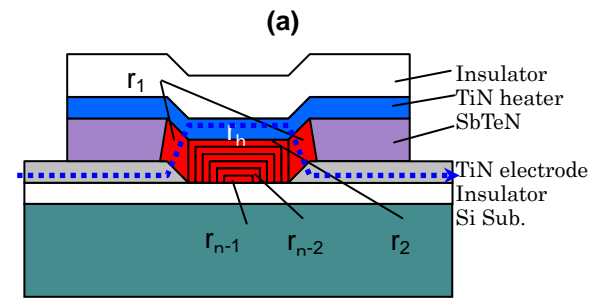


Fig. 5 Analysis of resistance switchings from (a) "0" to (b) "1" and then to (c) "2" on the basis of crystallization processes, which occurs at the steps due to electric field confinement effect.



**Principle for MLS**

$r_1 \rightarrow r_{1c}$  (Crystallization due to concentration of electric field)

$r_2 \rightarrow r_{2c}$  (Crystallization via Joule heating- 1)

⋮

$r_{n-2} \rightarrow r_{n-2c}$  (Crystallization via Joule heating-  $n-3$ )

$r_{n-1} \rightarrow r_{n-1c}$  (Crystallization via Joule heating-  $n-2$ )

Fig. 6 (a) Schematic cross-sectional diagram of our fabricated lateral PCM device with an additional top TiN heating layer. (b) Equivalent circuit and principle of the device for MLS.

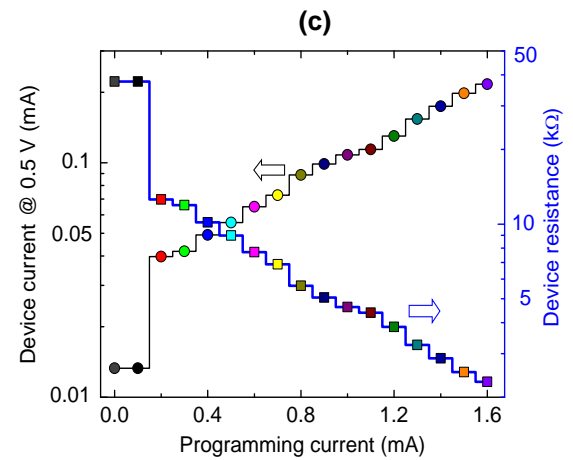
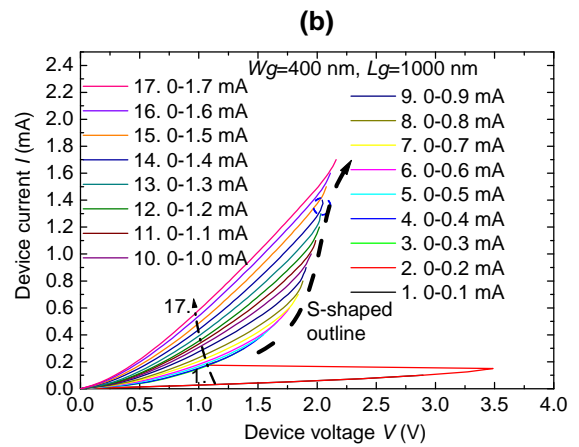
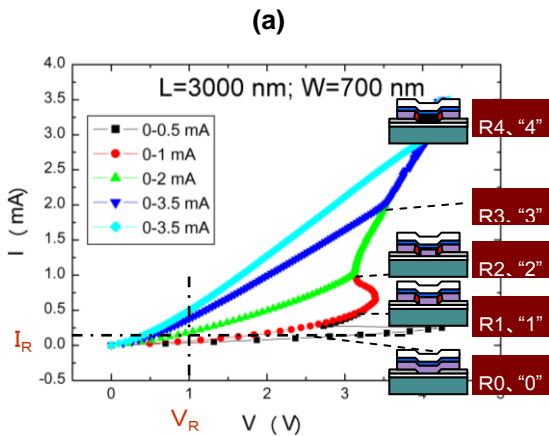


Fig. 7 (a) and (b) MLS programming by current sweep of the device for MLS at programming current intervals of 0.5-1.5 and 0.1 mA, respectively. (c) Relationship between resistance and programming current, showing staircase-like characteristics for MLS.

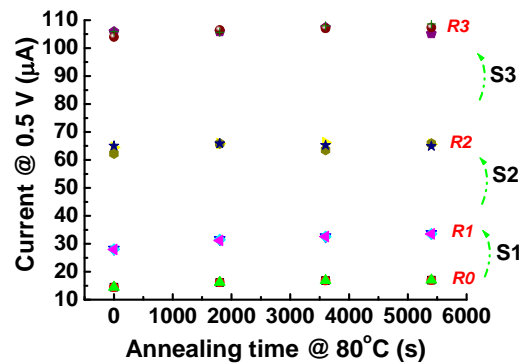


Fig. 8 Thermal stability at 80°C.