Feasibility study of $Ge_2Sb_2Te_5$/$GeCu_2Te_3$ memory cell with multi-level resistance

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ABSTRACT

In this work, as a feasibility study of multi-level resistance PCRAM, we investigated the phase change characteristics of $Ge_2Sb_2Te_5$(GST)/$GeCu_2Te_3$(GCT) memory cell. Since GCT shows lower meting and higher crystallization temperatures than GST, the direct transition for multi-level resistance states can be expected to be obtained. GST/GCT memory cell showed double switching phenomenon, which is due to the crystallization of GST layer and GCT layer. Moreover, after a higher and shorter reset pulse was applied to the memory cell, such double switching phenomenon was reconfirmed.
Key words: Ge-Cu-Te, Ge-Sb-Te, multi-level recording, multi-layer memory cell

1. INTRODUCTION

For high-density integration, the scaling-down of a cell size of phase change random access memory (PCRAM) has been widely studied. Moreover, the function of a multi-level recording is also essential to PCRAM like flash memory for high density. In the case of PCRAM having one phase change material, multiple states must be realized by adjusting set/reset pulse conditions. However, since one phase change material doesn't give a sufficient resistance margin for multi-level states in viewpoint of reliability, the structural innovation is needed [1, 2]. Meanwhile, the multi-level resistance PCRAM with two kinds of phase change materials has been proposed. However, for the combination using the conventional phase change materials like $Ge_2Sb_2Te_5$ (GST), Sb-Te-based alloy etc, since its melting point is proportional to its crystallization temperature, direct data transitions from original data to new data are impossible. In this work, as a feasibility study, we investigated the phase change characteristics of GST/ $GeCu_2Te_3$(GCT) memory cell. Since GCT shows lower meting and higher crystallization temperatures than GST [3, 4], the direct transition for multi-level resistance states is expected to be obtained.

2. MULTI-LEVEL OPERATION

Fig. 1(a) shows schematics of multi-level states (4 states) for PCRAM with serial connection of three kinds of phase change materials, M1, M2 and M3, where the resistance of amorphous state is higher in the order of M1, M2 and M3. Fig. 1 (b) and (c) show phase change and data transition characteristics of multiple phase change materials with different melting point and crystallization temperatures. Here, two cases can be discussed in viewpoint of phase change temperatures. In case of Fig. 1(b), M_1, M_2 and M_3 have high, middle and low crystallization temperatures, respectively, and high, middle and low melting points, respectively. Basically, since a phase change material with a higher crystallization temperature shows a higher melting point, the combination of phase change materials as shown in Fig. 1(b) is common case. In this case, troubles in some data writing happen. For example, to conduct the writing from "10" to "01", all materials must be crystallized first and then only M3 must be amorphized. Similarly, the

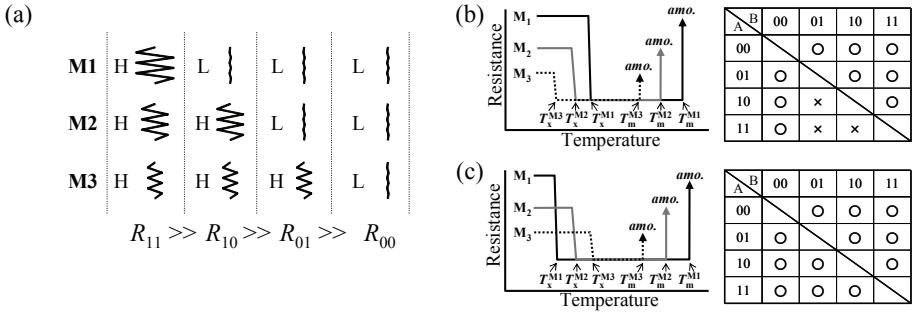

Fig.1. (a) Multi-level states in a combination of M1, M2 and M3 materials, where H and L mean high and low resistance, respectively. (b)(c) Combination of multiple phase change materials with different melting point and crystallization temperature. T_x and T_m indicate crystallization and melting temperatures. ×:direct transition (A→B) is impossible. ○:direct transition (A→B) is possible.

writing from “11” to “01” or “10” cannot be done directly. Such additional operation results in speed delay and power consumption in multi-level operation. Meanwhile, in a combination as shown in Fig. 1(c), a direct transition can be achieved because the materials show non-proportional relationship between melting point and crystallization temperature. As a feasibility study of a combination of Fig. 1(c), we investigated the phase change characteristics of GST/GCT memory cell.

3. EXPERIMENTS

TiN films with a thickness of 50 nm were used for medium and bottom electrode as a role of heater. The top and bottom phase change materials were GST and GCT, respectively. The contact area was 10 μm × 10 μm for both phase change materials. And, the top electrode was Al. The schematic of the device structure is shown in the inset of Fig. 2.

4. RESULTS AND DISCUSSION

Fig. 2 shows R-I curve of GST/GCT memory cell, where the inset shows the schematic of the device. The initial state of the both layers was amorphous. When a pulse current approaches to around 18 μA, the first resistance change from high to middle resistance is observed. And, when a pulse current increases to 70 μA, a change of an additional resistance is also observed, which shows data transition to lower resistance state. These results indicate that the middle states of “10” or “01” are directly achieved from “11” like Fig 1(c). Moreover, after a higher and shorter reset pulse was applied to the memory cell, such double switching phenomenon was reconfirmed [5]. Fig. 3 shows cyclic behaviors of the multi-layer cell. It was confirmed that transition from low- to middle-level, from middle- to low-level, from low- to high-level and from high- to low-level could be achieved by controlling the applying electrical pulse. These results suggest that the combination of GST/GCT gives better scaling feasibility to achieve gigabit array.

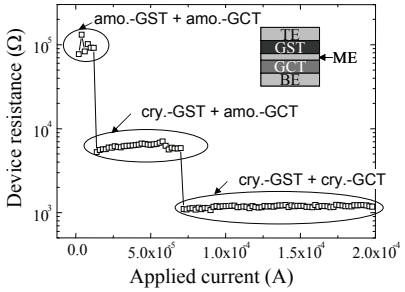

Fig.2. R-I characteristic of memory cell with GST and GCT. Here, three resistance states are confirmed. TE, ME and BE indicate top, middle and bottom electrodes.

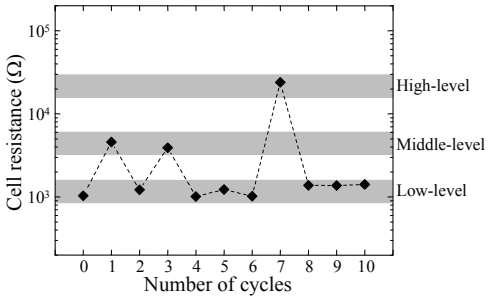

Fig.3. Cyclic characteristic of the multi-layer cell. Three-state transition was confirmed by controlling the applying electrical pulse.

5. CONCLUSION

Multi-layer device with GST and GCT showed multi-resistance level state. The present results suggest that the GCT can be one of candidate materials for a middle or low data state in multi-level PCRAM cell providing a direct transition without any additional step during writing operation. Such a multi-level PCRAM cell is expected to show high speed operation and low power consumption.

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