Low-Power Super-Lattice Phase-Change Memory without Melting and Write-Pulse Down Slope

Koh Johguchi, Toru Egami and Ken Takeuchi
Department of Electrical, Electronic, and Communication Engineering, Chuo University, Tokyo, Japan

I. Introduction

Phase change memory (PCM) is one of the promising candidates for the next generation storage memory due to its high speed and low energy consumption [1]. A $Ge_2Sb_2Te_5$ (GST) film is often used as the phase change material and requires proper heat control because the quenching speed determines amorphization (RESET) or crystallization (SET). Therefore, it is important for a PCM to control the pulse down slope, which is difficult due to large BL parasitic parameters. Additionally since Joule heating is used to change the state, the thermal disturb [2] and the electro-migration (EM) due to large write-current are critical issues for the reliability of scaled devices. Thus a super-lattice PCM (SL-PCM) has been developed for further scaling and reliable operation [3-6]. In SL-PCM, a meta-material structure composed of GeTe and SbTe layers is used for the phase change material, and SET or RESET operations are carried out by Ge atom flip-flop transition [4, 5]. Therefore, the SL-PCM is not melted during phase change and unnecessary energy consumption, which is as previously dissipated as Joule heating, can be saved.

II. Measurement results

Fig. 1 depicts the experimental comparison results between the conventional GST- and SL-PCMs. The measurement results show that the energy dissipation of SL-PCM is less then ×0.1-×0.01 that of the conventional GST due to the efficient resister switching. Fig. 2(a) shows the SET pulse width (T_{pw}) dependence of a 300-nm SL-PCM device. 100 ns pulse width is needed for SET complete. Although SET is complete when $T_{pw} > 100$ ns, the optimum SET condition is $T_{pw} = 100$ ns since too long SET pulse causes large energy dissipation. Fig. 2(b) gives the pulse slope dependency of SET operation. If T_f is too long, not only the energy is wasted but the resistance may change to RESET state again after SET complete (SET disturb) unlike the conventional $Ge_2Sb_2Te_5$ PCM. In other word, too long pulse slope causes SET failure [8]. Therefore, for SL-PCM, the pulse slope becomes a factor contributing to disturb in SET operation. From this result, it is found that SL-PCM does not melt during SET [4, 5] and the conductivity of SL-PCM is caused not by Joule heating but by Ge-atom transition. In addition, the retention-time is measured at high-temperature

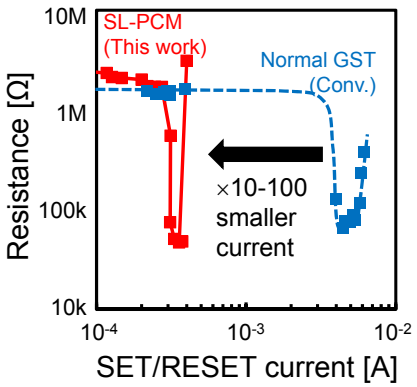
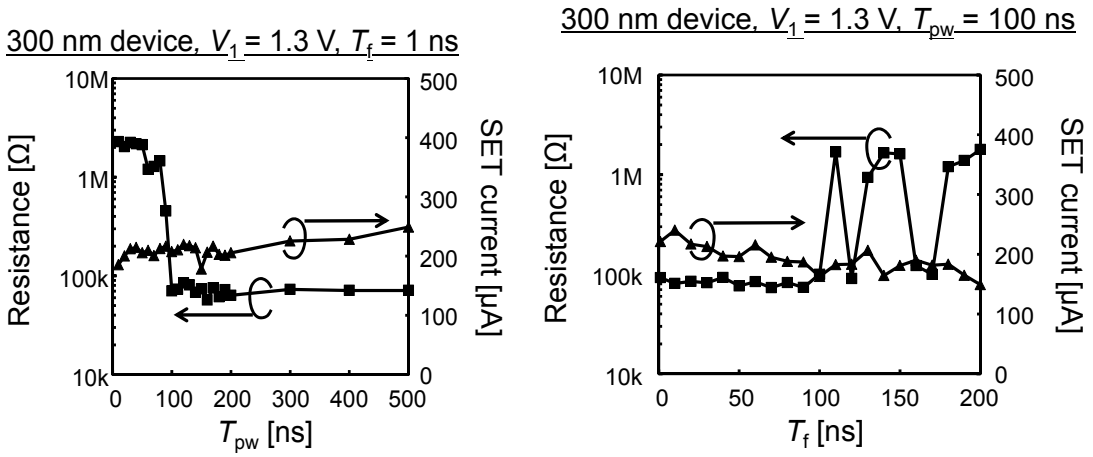


Fig. 1 SET/RESET characteristics of SL-PCM and the conventional GST.

(HT = 85 ºC) to evaluate the reliability of SL-PCM. Even at HT, over 10^5 sec of data retention time is achieved. The read disturb problem is also verified with V_{read} = 0.3 V and T_{read} = 100 ns. From the measurement results, the read disturb is insignificant for data retention.



(a) (b)

Fig. 2 (a) SET pulse width (T_{pw}) and (b) pulse down slope (T_f) dependence with T_{pw} = 100 ns.

III. Conclusions

A low power, high reliability SL-PCM is measured and investigated. The measurement results show that the pulse falling edge of SET is ineffective and that SET is not dependent on Joule heating. This result suggests the state transition of SL-PCM is carried out not by melting, but by a Ge flip-flop, which can provide low-power operation and simpler write circuit with reliability. Moreover, the temperature dependencies of SL-PCM are investigated. As the temperature rises, the conductivity increases which makes the SET operation easier while the RESET condition becomes more difficult. Positive retention-time and read-disturb test results also indicate potential as a future storage device.

Acknowledgement

This work was done in “Ultra-Low Voltage Device Project" of LEAP and supported by METI and NEDO

References

[1] R. Bez, *Dig. Tech. Papers, IEEE IEDM*, pp. 89-92, 2009. [2] S.B. Kim, *et. al.*, *Proc. IEEE IRPS*, pp. 100-103, 2010. [3] H.X. Yang, *et. al.*, *Proc. IEEE IMW*, pp. 68–69, 2009. [4] J. Tominaga, *et. al.*, *Jpn. J. Appl. Phys.*, vol. 47, pp. 5763-5766, 2008. [5] J. Tominaga, *et. al.*, *Proc.E¥PCOS*, 2010. [6] T. Shintani, *et. al.*, *Proc. E¥PCOS*, 2011. [7] A. Cabrini, *et. al.*, *Proc. ICECS*, pp. 186-189, 2008. [7] S. Lee, *et. al*, *Appl. Phys. Lett.*, vol. 95, 093504, 2009. [8] K. Johguchi, *et. al.*, *Proc. IRPS*, 2013.

.