Low-Power Switching in Phase-Change Memory using New Superlattice : SnTe/Sb_2Te_3 System

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ABSTRACT

A new material SnTe for a superlattice (SL) phase-change device is proposed as the substitute of GeTe. XRD results showed that a SnTe(111)/Sb_2Te_3(001) SL formed, though SnSbTe-alloy peaks were greatly dominant. The switching power of this device was approximately 1/10th－1/15th that of a $Ge_2Sb_2Te_5$ device, and, almost equivalent to or lower than that of a GeTe/Sb_2Te_3 SL device. The endurance was confirmed to be higher than 10^5 cycles. For the mechanism of the low switching power, Sn switching might work. This is, however, still a supposition.

Key words: phase-change memory, superlattice, interfacial phase-change memory (iPCM), SnTe/Sb_2Te_3

1. INTRODUCTION

A phase-change random access memory is expected to be next generation non-volatile solid-state memory[1]. The most urgent issue of phase-change memory for commercialization is the reduction of switching power for resistance switching. Recently, "interfacial phase-change memory" (iPCM) composed of a GeTe(111)/Sb_2Te_3(001) superlattice (SL) has been proposed, and verified to suppress the switching power drastically[2]. In such a SL, Ge atoms reversibly switch between octahedral and tetrahedral sites in GeTe-lattice depending on applied voltage and/or current. This mechanism has been confirmed with both the theoretical first principle calculation[3] and experiment[2]. This type of iPCM is a strong candidate as the recording material for the future phase-change memory.

This article proposes a new SL material SnTe/Sb_2Te_3 for low-power switching of a phase-change memory. The experimental results on this SL are reported and discussed. A further direction of this study is also included.

2. EXPERIMENT

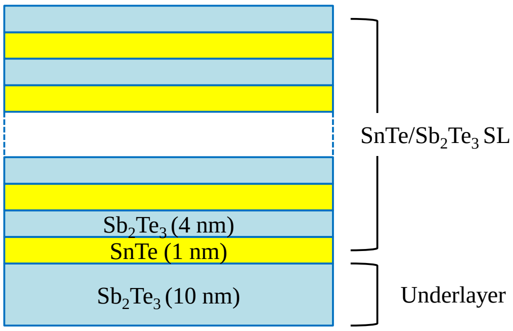

Figure 1 Schematic illustration of SnTe/Sb_2Te_3 SL structure.

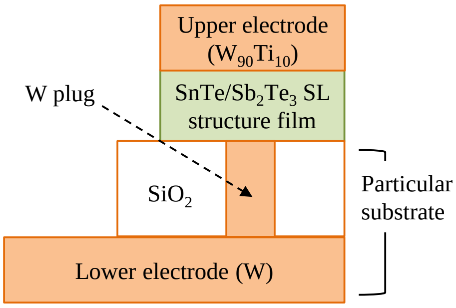

Figure 2 Schematic illustration of SnTe/Sb_2Te_3 SL device.

Two kinds of substrates were used: glass for XRD experiment and particular substrate described in Ref. 4 for fabrication of the SnTe/Sb_2Te_3 SL device. The film structure on these substrates was as follows: Sb_2Te_3(10 nm) / [SnTe (1 nm) / Sb_2Te_3 (4 nm)]$_9$ /$W_{90}Ti_{10}$ (50 nm), which is shown in Figs. 1 and 2. All the films were deposited by using a magnetron sputtering apparatus. The substrate temperatures were room temperature for $W_{90}Ti_{10}$ film as a top electrode, and 200℃ for each chalcogenide film. Using photolithography, the SL device shown in Fig. 2 was fabricated.

XRD experiments were carried out to identify the phases of sputter-deposited films and to investigate their crystalline orientations. A prober apparatus was used to investigate the electrical properties of the SL device.

3. RESULTS

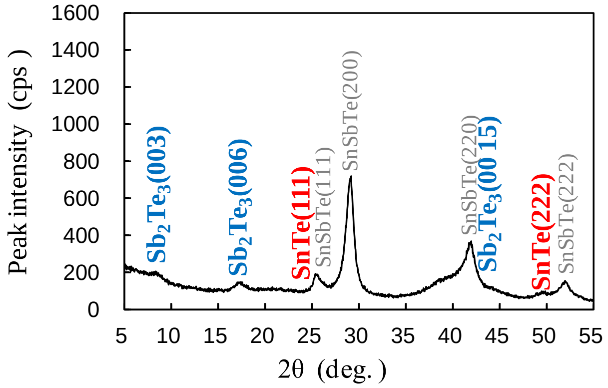

Figure 3 XRD profile of SnTe/Sb_2Te_3 SL film.

Figure 3 shows the XRD profile for the SnTe/Sb_2Te_3 SL film. Small SnTe(111) and (222), and $Sb_2Te_3(00l)$ (l : 3, 6, and 15) peaks were observed with strong SnSbTe-alloy’s peaks. These results showed that a SnTe(111)/Sb_2Te_3(001) SL phase formed and that SnSbTe-alloy phase dominantly formed.

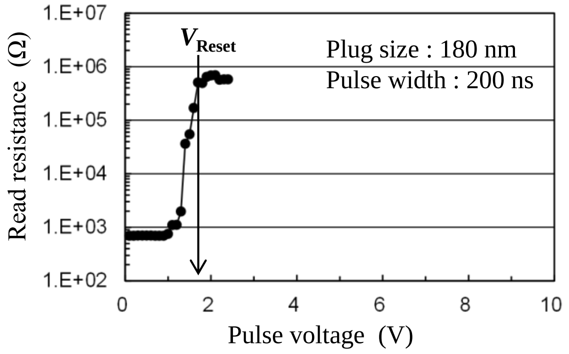

Figure 4 Dependence of the read resistance on the pulse voltage for the SnTe/Sb_2Te_3 SL device.

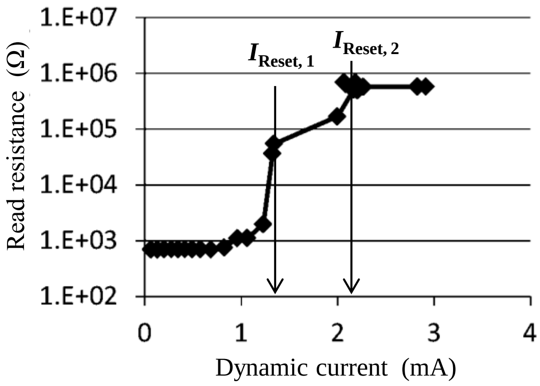

Figure 5 Dependence of the read resistance on the dynamic current.

Figure 4 shows the dependence of the read resistance on the pulse voltage for the SnTe/Sb_2Te_3 SL device. The set (reset) voltage was less than 0.1 V (about 1.7 V). Figure 5 shows the dependence of the read resistance on the dynamic current. In Fig. 5, the two-step changes in resistance were observed. In this stage, we cannot determine which is true as the reset current. When we define two reset currents $I_{\mathrm{Reset,\,1}}$ and $I_{\mathrm{Reset,\,2}}$, the $I_{\mathrm{Resst,\,1}}$ (I_{Reset2}) was about 1.4 mA (2.1 mA). Multiplying the above reset voltage by this $I_{\mathrm{Reset,\,1}}$ ($I_{\mathrm{Reset,\,2}}$), the switching power: the consumed power which was defined with the reset power was about 2.4 mW (3.6 mW). Since the switching power of a $Ge_2Sb_2Te_5$ device (a GeTe/Sb_2Te_3 SL device) was about 36 mW (3.6 mW)[4] with the same prober, this power is approximately 1/10th－1/15th that of a $Ge_2Sb_2Te_5$ device[4], and almost equal to or lower than that of a GeTe/Sb_2Te_3 SL device[4].

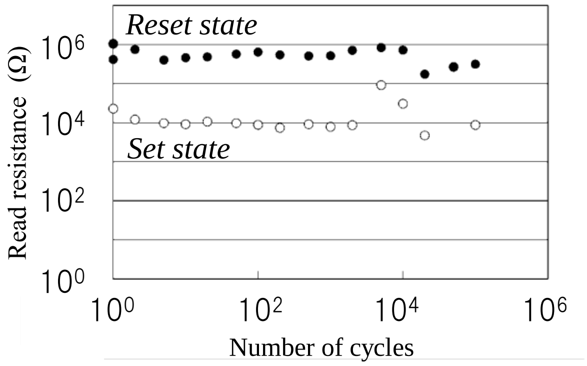

Figure 6 Endurance of SnTe/Sb_2Te_3 SL device.

Figure 6 shows the data on endurance of the SnTe/Sb_2Te_3 SL device. At least 10^5 cycles were confirmed, though resistance fluctuations were observed during the 10^3 – 10^4 cycles.

4. DISCUSSIONS

The mechanism of low switching power (Figs. 4 and 5) in the SnTe/Sb_2Te_3 SL device is not clear. Considering the following three matters: (1) Sn is one row under Ge in the Periodic Table, (2) Both GeTe and SnTe have the same NaCl-type crystalline structure, and (3) Ref. 5 mentions that Sn increases the mobility of the atoms in Sn-doped $Ge_2Sb_2Te_5$ film, the same phenomenon as GeTe/Sb_2Te_3 SL device, i.e., Sn switching (6 fold bond⇔4 fold bond switching) might work[2,3]. This is, however, still a supposition.

The two-step changes in resistance in Fig. 5 and the resistance fluctuations in Fig. 6 might be due to the low-quality sputtered films. The SnSbTe-alloy phase dominates the films (Fig. 3). The alloy phase is considered to be formed through the following processes: The nucleus formation was produced with large lattice mismatch between the SnTe and Sb_2Te_3 (～5.4 %) and subsequent grain growth was produced with too high substrate temperature (200℃) to obtain crystalline SnTe film. (Crystallization temperature of SnTe＜room temperature.) Thus, the amount of the alloy phase must be reduced by decreasing the substrate temperature, leading to solve the problems of the two-step changes and the resistance fluctuations.

5. CONCLUSION

We demonstrated that the SnTe/Sb_2Te_3 SL device shows the low-power resistance switching. The switching power was approximately 1/10th－1/15th that of a $Ge_2Sb_2Te_5$ device, and, almost equivalent to or lower than that of a

GeTe/Sb_2Te_3 SL device. The endurance was confirmed to be higher than 10^5 cycles. The SnTe/Sb_2Te_3 SL device might be candidate for future phase-change memory.

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