Hybrid Memory Architecture of PCM and NAND Flash Memories for Enterprise Storage

Ken Takeuchi

Dept. of Electrical, Electronic and Communication Engineering
Chuo University, Tokyo, Japan
E-mail : takeuchi@takeuchi-lab.org, URL : http://www.takeuchi-lab.org

SSDs and emerging storage class non-volatile semiconductor memories (SCM) such as PCRAM, FeRAM, ReRAM and MRAM have enabled innovations in various nano-scale VLSI memory systems for personal computers, multimedia applications and enterprise servers [1]. This paper provides a comprehensive review on state-of-the-art data management technologies of storage class memory and NAND flash memory hybrid solid-state drives (SSDs). A 3D through-silicon-via (TSV)-integrated hybrid PCM/multi-level-cell (MLC) NAND solid-state drives' (SSDs') architecture is proposed for PC, server and smart phone applications [1]. NAND-like interface (I/F) and sector-access overwrite policy are proposed for PCM. Furthermore, intelligent data management algorithms are proposed. The proposed algorithms suppress data fragmentation and excess usage of the MLC NAND by storing hot data in the PCM. As a result, 11 times performance increase, 6.9 times endurance enhancement and 93% write energy reduction are achieved compared with the conventional MLC NAND SSD. Both PCM write and read latency should be less than 3us to obtain these improvements. The required endurance for PCM is 10k cycles. 3D TSV interconnects reduce the energy consumption by 68%.

References

[1] Ken Takeuchi, "Novel Co-design of NAND Flash Memory and NAND Flash Controller Circuits for sub-30nm Low-Power High-Speed Solid-State Drives (SSD)," IEEE Symp. on VLSI Circuits, pp.124-125, June 2008.

[2] Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi, Chao Sun and Ken Takeuchi, "x11 Performance Increase, x6.9 Endurance Enhancement, 93% Energy Reduction of 3D TSV-Integrated Hybrid ReRAM/MLC NAND SSDs by Data Fragmentation Suppression," IEEE Symp. on VLSI Circuits, pp.134-135, June 2012.