Current-driven crystallization promotion for multilevel storage in phase-change memory

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ABSTRACT

In this study, we report current-driven crystallization promotion for multilevel storage in both lateral and vertical phase-change memories (PCMs). For the lateral device, the active medium consists of a top 50-nm TiN/150-nm SbTeN. It was demonstrated that the number of distinguishable resistance levels can readily reach 16 and even higher. For the vertical device, $TiSi_3/Ge_2Sb_2Te_5/TiN$ structure was adopted and 8 distinct resistance levels were demonstrated. These resistance levels in this study result from the initial threshold switching and the subsequent current-driven crystallization promotion induced by Joule heating.

Keywords Multi-level storage, Crystallization promotion, Phase-change memory

INTRODUCTION

To increase the memory capacity without further increasing cost, researchers have focused their attention on multilevel storage (MLS), which is data storage of more than two levels per memory cell.[1)] In recent years, MLS has been demonstrated in both conventional and emerging memories, such as flash memory, phase-change memory (PCM),[2-4)] and resistive random access memory (RRAM). However, flash memory itself has many demerits and the mechanism of RRAM is still not understood very well. And MLS was demonstrated by using multilayer structures or the properties of phase-change materials with different phase-change temperatures. But the available number of resistance levels is strictly dependent on the number of multilayers or the phase-change temperatures.

Although MLS with more than 8 resistance levels was demonstrated by some groups such as IBM based on high-power amorphization, [5)] there is a lack of study on MLS based on low-power crystallization. In this study, we report the control of resistance realized mainly through the gradual enlargement of the crystallization region induced by current-driven Joule heating using a lateral and a vertical structures and 8-16 resistance levels are demonstrated using this method.

RESULTS AND DISCUSSIONS

1. Lateral device

The active layers of the device consist of 150-nm-thick SbTeN[6)] layer and an additional top 50-nm-thick TiN layer as shown in Fig. 1(a). Fig. 1(b) shows our concept of MLS based on filament formation, crystallization and the subsequent enlargement of the crystalline zone (e.g., n resistance levels here).

Fig. 2(a) shows the programming characteristics of the device by current sweepings from 0 to the programming currents I_p. The programming currents were 0.5, 1, 2, and 3.5 mA, respectively. It can be observed that the intermediate levels were very stable because the changed resistance levels can be retained until the sweeping current became higher than the former programming current. In particular, the resistance can be determined by the stop current. It should be

noted that more intermediate levels are possible by reducing the programming current interval, as shown in Fig. 2 (b). The resistance-programming current (R-I_p) curve in Fig. 2(c) shows the possibility of 16-level storage. Stability of the resistance levels created by crysatallization promotion shown in Fig. 3.

2. Vertical device

A cross section of our vertical device is schematically shown in Fig. 4.[7] The crystallization (C-GST) promoted with increasing amplitude of programming currents in our device was investigated on the basis of finite element analysis, as shown in Fig. 5. Figure 6(a) shows the shifted current-voltage (I-V) curves of Sn (n=1–8) when the current was swept between the electrodes. We first swept the device current forward from 0 to the maximum current I_{max1} of 0.2 mA and backward from 0.2 to 0 mA. The I-V curve corresponds to S1 in Fig. 6(a). Then, we increased the maximum current to 0.3 mA (I_{max2}) and swept the current from 0 to 0.3 mA and then back to 0 mA. The measured I-V curve corresponds to S2 in Fig. 4(a). Similarly, we gradually increased the maximum currents to 0.5mA (I_{max3}), and finally to 3.5 mA (I_{max8}), and the I-V curves of S3, S4, S5, S6, S7 and S8 were measured. All of these curves are shown in Fig. 6(b) without any shift.

The device resistances read at a low current with increasing programming currents are shown in Fig. 6(c). These subsequent gradual resistance drops resulted from the enlargement of the crystalline region, as shown in Fig. 5(a). 8 distinct and stable resistance levels were created here, and they were induced by current-driven programming. These discrete resistance levels corresponding to crystallization regions of different sizes were determined by the programming currents.

CONCLUTIONS

A lateral SbTeN-based PCM device with a top TiN heating layer and a vertical $TiSi_3$/$Ge_2Sb_2Te_5$/TiN device were proposed and investigated for multilevel storage. Current-driven crystallization promotion was demonstrated for ultra-multiple-level storage. The crystallization induced by Joule heating is non-volatile, low-power and current-driven, and allows ultra-multiple-level storage. This phenomenon is expected to be employed in practical applications to dramatically increase the memory capacity without increasing the cell size.

ACKNOWLEDGEMENTS

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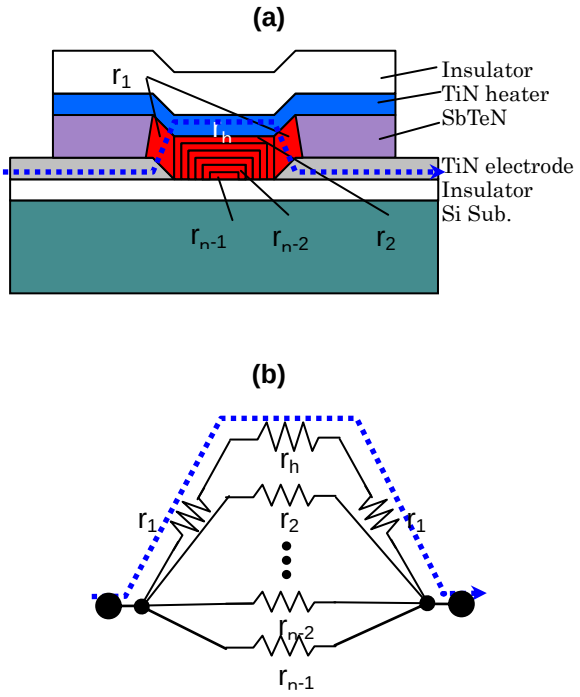
REFERENCES

1. Y. Yin, N. Higano, H. Sone, and S. Hosaka, *Appl. Phys. Lett*. **92** (2008) 163509.
2. S. R. Ovshinsky, Jpn. J. Appl. Phys. **43** (2004) 4695.
3. Y. Yin, K. Ota, T. Noguchi, H. Ohno, H. Sone, and S. Hosaka, *Jpn. J. Appl. Phys*. **48** (2009) 04C063.
4. Y. Yin, and S. Hosaka, *Appl. Phys. Lett*. **100** (2012) 253503.
5. Y. C. Chen, C. T. Rettner, S. Raoux, G. W. Burr, S. H. Chen, R. M. Shelby, M. Salinga, et al., *Tech. Dig. IEDM*, 2006, p. 777.
6. Y. Yin, H. Sone, and S. Hosaka, *J. Appl. Phys*. **102** (2007) 064503.
7. Y. Yin, and S. Hosaka, *Jpn. J. Appl. Phys*. **51** (2012) 064101.



Principle for MLS

$r_1 \rightarrow r_{1c}$ (Crystallization due to concentration of electric field)

$r_2 \rightarrow r_{2c}$ (Crystallization via *Joule heating- 1*)

$r_{n-2} \rightarrow r_{n-2c}$ (Crystallization via *Joule heating- n-3*)

$r_{n-1} \rightarrow r_{n-1c}$ (Crystallization via *Joule heating- n-2*)

Fig. 1 (a) Schematic cross-sectional diagram of our fabricated lateral PCM device with an additional top TiN heating layer. (b) Equivalent circuit and principle of the device for MLS.

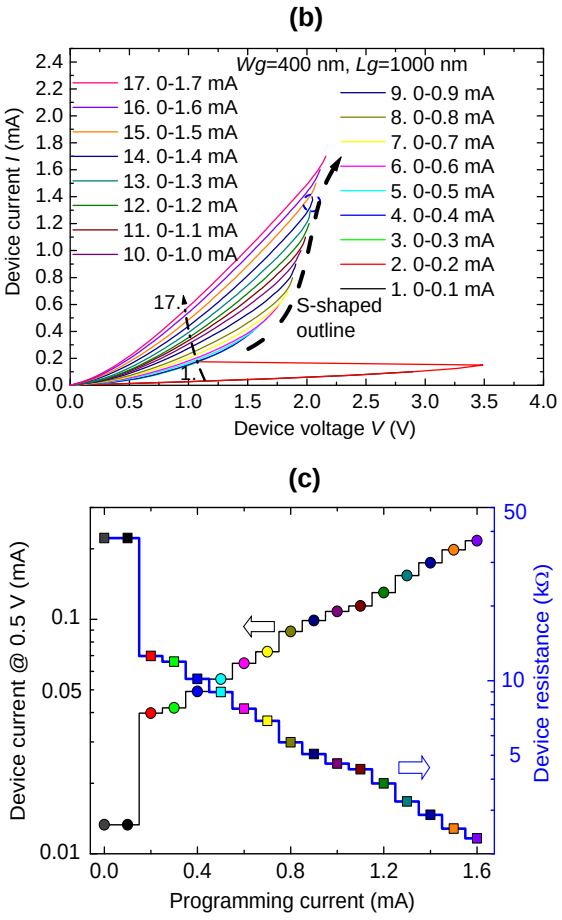
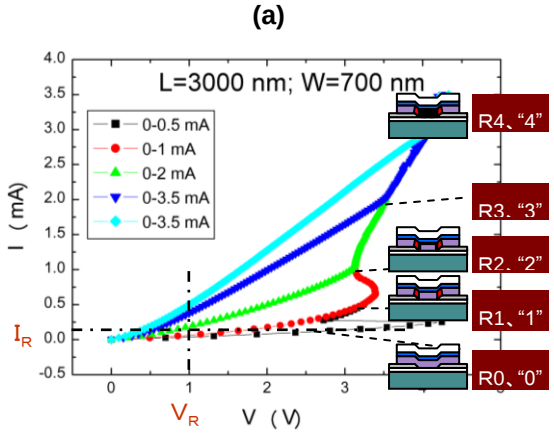


Fig. 2 (a) and (b) MLS programming by current sweep of the device for MLS at programming current intervals of 0.5-1.5 and 0.1 mA, respectively. (c) Relationship between resistance and programming current, showing staircase-like characteristics for MLS.



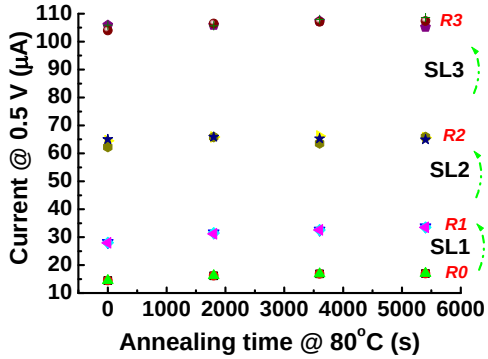


Fig. 3 Thermal stability at 80°C.

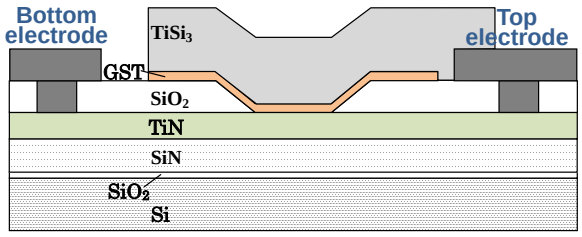


Fig. 4 Schematic cross-sectional diagram of our fabricated vertical PCM device.

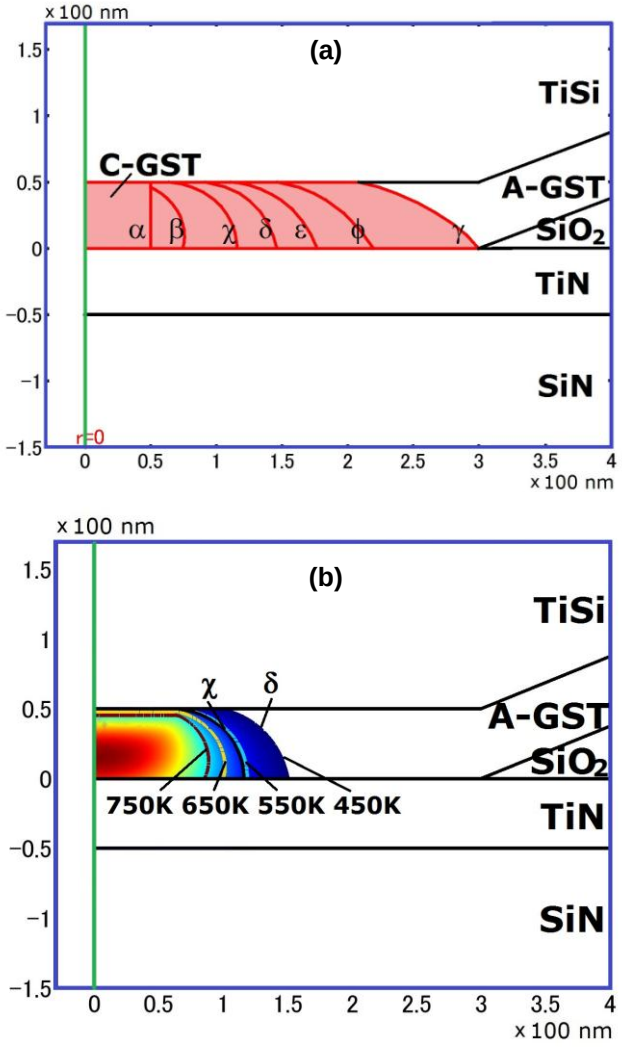


Fig. 5 (a) Simulated crystallization promotion based on finite element analysis. Crystallization begins with a filament formation with an outline of α. Crystallization then proceeds from β to χ, δ, ε, ϕ, and finally to γ. (b) Temperature distribution of GST when a pulse is applied. The outline of crystallized area changes from χ to δ.

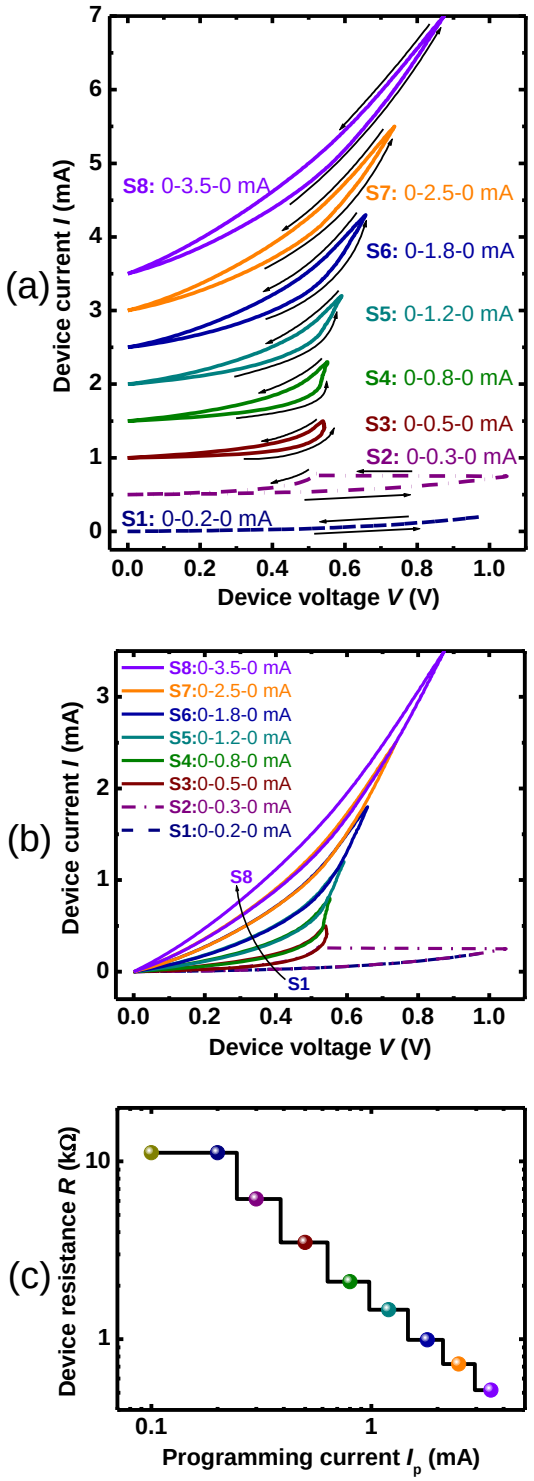


Fig. 6 multilevel storage in the fabricated device. (a) Shifted *I-V* curves when the current was swept forward from 0 mA to the programming current and backward from the programming current to 0 mA. (b) *I-V* curves without any shift exhibit an S-shaped outline due to the resistance changes. (c) Device resistance vs programming current showing eight resistance levels.