Scalable High Performance PRAM for Storage Class Memory

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ABSTRACT

The required properties of SCM are high read/write performance and superior cycling endurance. By adopting the 20nm confined cell, we were able to reduce the RESET current below 100uA using doped TiN heater. tSET was enhanced 5times (~150ns) using optimized GeSbTe composition. Also, endurance cycles were improved up to 10^{11} cycles even under higher programming current stress. Our results indicated that the 20nm confined cell structure with optimized GeSbTe is applicable to the Storage Class Memory (SCM) application and Hybrid SSD system possibilities for PRAM.

Key words: PRAM, Storage Class Memory (SCM), SSD, RESET Current, tSET, Endurance

1. INTRODUCTION

The widespread use of NAND flash memories in SSDs has unleashed new avenues of innovation for the enterprise and client computing. The system-wide architectural changes are required to make full use of the advantages of SSDs in terms of performance, reliability and power as shown in Figure 1. SCM is used as write buffers as shown in Figure 2. At the 10 Gbps write, the proposed SSD decreases the power consumption by 97%[1]. Especially, the emerging storage class memories (SCM) such as PRAM, RRAM and MRAM are becoming a viable alternative to commonly used volatile and nonvolatile memories. Being bit-alterable like DRAM and nonvolatile like a flash memory together with CMOS-process compatibility, these non-volatile random access memories have a potential to revolutionize various aspects of the computing platform architectures [2]. These resistive memories are more scalable than conventional memories since resistive information can be stored in a few nm size cells and almost free from leakage. Among the resistive memories, PRAM has been widely investigated as not only non-volatile memory but also high performance SCM. In this paper, we describe the key metrics and possible solutions for SCM in the 20nm technology node PRAM.

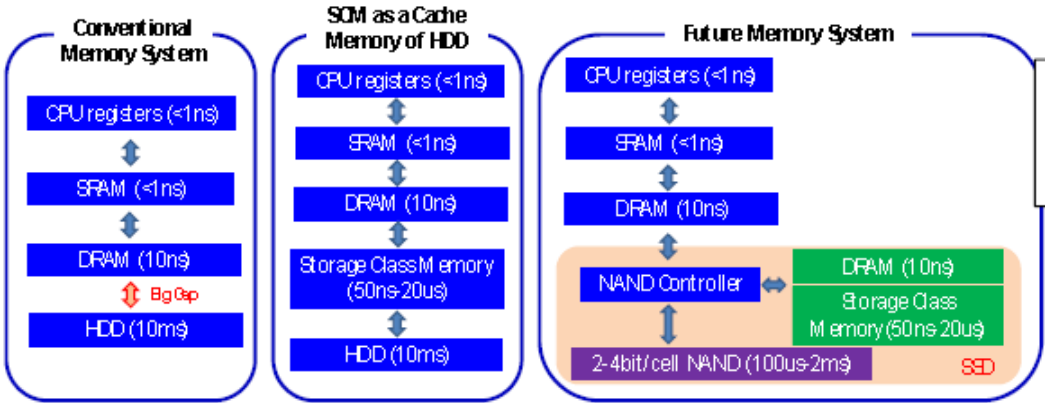

Fig. 1 Conventional and future SCM & NAND flash memory hybrid memory system [1].

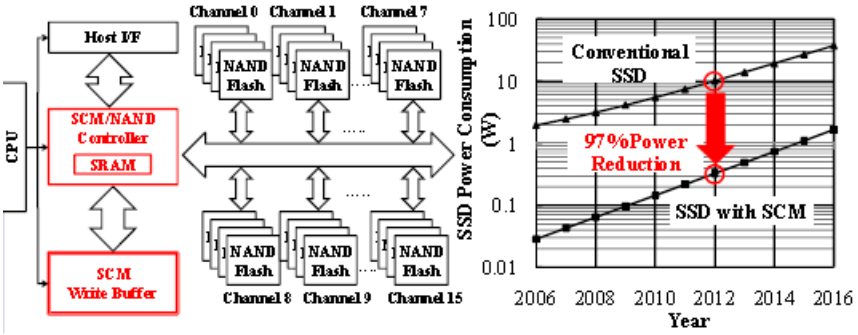

Fig. 2 SCM & NAND flash memory hybrid SSD system [1].

2. RESET Current Scaling

RESET current reduction is one of the key issues for high data rate in high performance PRAM. Two approaches have been developed to reduce the RESET current. One is to increase the resistance of heating elements by contact dimension scaling or resistivity increasing. The other is to improve heat efficiency by reducing a required programming volume. In order to dramatic decrease of RESET current, combination of two approaches are essential. Fig. 3 show the TEM images of 20 nm size confined cell and temperature profile of confined cell along BL and WL directions, respectively [3]. Fig. 4 shows the R-I curve of 20 nm confined cell, which successfully reduced the RESET current below 100uA using doped TiN heater.

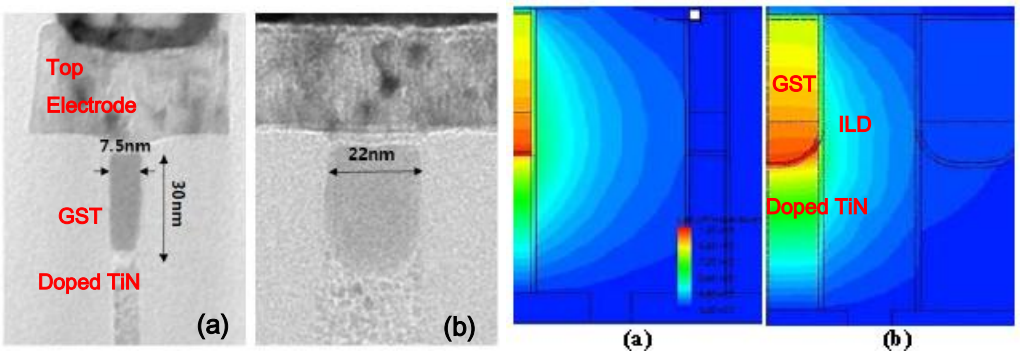

Fig. 3 Cross sectional TEM images of 20nm confined cell and temperature profile of confined cell along BL direction (a) WL direction and (b) BL direction.

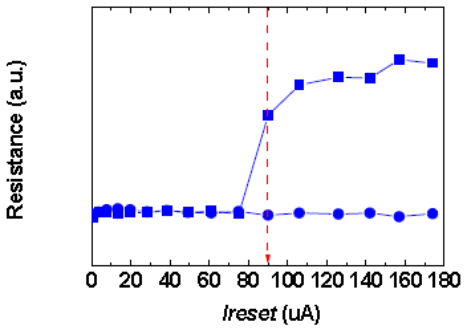

Fig. 4 Resistance-Current curve of 20nm confined cell.

4. Write Performance

Write speed of PRAM is mostly dependent on the crystallization time of phase change materials. GST based materials such as $Ge_2Sb_2Te_5$, $Ge_1Sb_2Te_4$ and $Ge_1Sb_4Te_7$ shows crystallization above 30~300 nano seconds. Fig. 5 shows the measured write performance of integrated 20nm PRAM cell [4], where the pulse of 150ns duration (tSET) is sufficient to crystallize the PRAM cell to “SET” state. tSET was enhanced 5times using optimized GeSbTe composition. In addition to the improved program time (tPGM), the reset

current (IRESET), and accordingly, the program current (IPGM) is also reduced around 100μA. To take advantage of the reduced IPGM, 128b parallel write operation is performed, compared to the 32b parallel write operation of the previous work [5]. Consequently, the write performance of this work is improved to 40 MB/s, which enables about 6× write-throughput improvement. When an external high voltage is applied, the write bandwidth can be extended as high as 133MB/s.

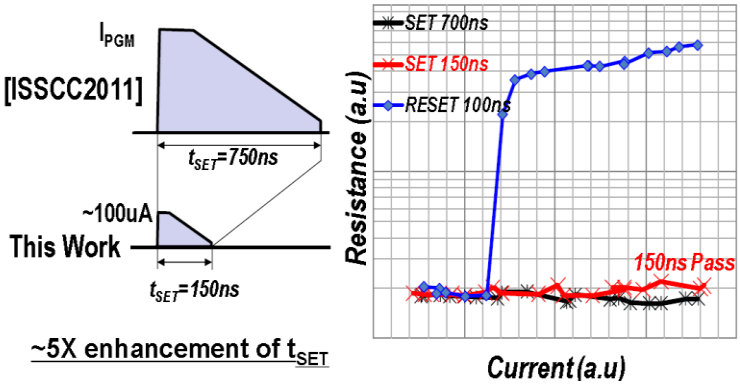

Fig. 5 Resistance-current curve of 20nm confined cell as a function of tSET.

3. Endurance cycles

Phase change is conducted through joule heating at the memory volume via current pulses. The instantaneous temperatures in the memory cell itself and at the interface in contact with heater electrode reach beyond 700C. At such high temperature, cycling endurance might be failed due to contact delimitation, material intermixing between memory material and the contact heater. Both voiding and compositional changes are affected from the bias dependent atomic transport due to electro-migration in the molten GST and/or incongruent melting occurred at the boundary region of liquid and solid phases. Fig.7 shows that the endurance can be improved by modifying the programming structure in which confined cell structure was fabricated, resulting in complete melting cell structure [6]. It was found that the endurance cycles were improved up to 10^{11} cycles even under higher programming current stress. This means that local incongruent melting can be avoided by utilizing complete volume melting cell structure.

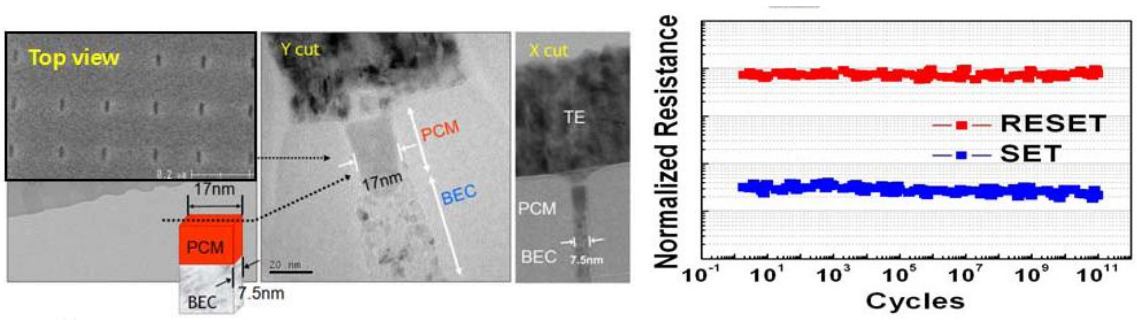

Fig. 6 Confined cell structure was shown. The memory volume was fully isolated in confined cell structure. And its endurance characteristics showed no failure until 10^{11}cycles.

4. CONCLUSION

We successfully integrated 20nm confined cell structure. Adopting the 20nm confined cell, we were able to reduce the RESET current below 100uA using doped TiN heater and tSET was enhanced 5times (~150ns) using optimized GeSbTe composition. Also, endurance cycles were improved up to 10^{11} cycles even under higher programming current stress. In this paper, could be a key to opening up the SCM application and Hybrid SSD system possibilities for PRAM. Finally, we presented an 8Gb PRAM with 40MB/s write

bandwidth featuring 8Mb sub-array core architecture with 20nm diode-switched PRAM cells. When an external high voltage is applied, the write bandwidth can be extended as high as 133MB/s.

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